

Inventors: DENNIS, Jack et al.
Serial No. 09/833,578

PATENT APPLICATION
Navy Case 84,886

Remarks

Claims 46-53 are pending in the present application. The specification and claims 11, 36 and 41 were objected to for minor informalities, as described in paragraphs 1 and 2 of the Office action. Claims 15 and 20 were rejected under 35 U.S.C. § 112, second paragraph, as described in paragraph 4 of the Office action. Claims 1-45 were rejected under 35 U.S.C. § 102(b), as described in paragraph 6 of the Office action. Claims 46 and 51 are the only independent claims.

The specification has been amended to correct minor typographical errors, including that which is discussed in paragraph 1 of the Office action. Accordingly, it is respectfully requested that the objection to the disclosure be withdrawn.

It is respectfully submitted that the outstanding objections and rejections are moot, as claims 1-45 have been cancelled.

In the prior art, as discussed in the paragraphs [0026] and [0027] of the present application, problems arise when multiple processors are intended to access shared resources. First, latency inherent in accessing shared resources results in lower processing speed. Second, because of the related nature of network data elements, conflict can occur between processing elements for access to shared resources. Consider, for example, a first processing element and a second processing element that are accessing the same shared variable. Suppose that the first processor accesses the shared variable, changes it, and initiates a storage operation to store the new value to memory. Because of latency and other timing issues, the second processing element may, while the first processing element is manipulating the shared variable, retrieve an invalid copy of the shared variable. Consequently, processing the invalid copy of the shared variable leads to corrupted data.

The present invention addresses the above-discussed problems associated with the prior art.

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In accordance with one aspect of the invention, a first processing element writes data to a shared resource. In addition to writing the data to the shared resource, the data is forwarded to a second processing element. As a result of this aspect, the second processing element is able to use the forwarded data immediately, rather than retrieving the data from the shared resource, thus eliminating time delay due to latency. As a further result of this aspect, the second processing element is able to compare the data in the shared resource and the data that has been forwarded to determine which copy of the data is to be used for processing. As such, this procedure avoids processing of an invalid copy of shared data. This aspect is described in the specification, for example, starting at paragraph [0093] with reference to FIGs. 9 and 10, and is recited in each of the independent claims.

Newly added independent claim 46 is drawn to a data processing apparatus comprising a first processing element, a forwarding storage element and a second processing element. Further, the first processing element is required to be operable to send first data to a resource and to send second data to the forwarding storage element, wherein each of the first data and second data corresponds to original data. Still further, the second processing element is required to be operable to attempt to access the first data in the resource and to attempt to access the second data in the forwarding storage element. Finally, claim 46 recites that:

“when said second processing element accesses the first data in the resource and accesses the second data in the forwarding storage element, and when it is determined that the first data in the resource and the second data in said forwarding storage element are not the same, said second processing element uses the second data from said forwarding storage element.”

Newly added independent claim 51 is drawn to data processing method comprising sending first data, which corresponds to original data, from a first processing element to a resource and sending second data, which corresponds to the original data, from the first processing element to a forwarding storage element. The method further comprises accessing, via a second processing element, the first data in the resource and accessing, via the second processing element, the second data in the forwarding storage element. The method still further

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comprises determining whether the first data in the resource and the second data in the forwarding storage element are not the same. Finally, the method comprises

“using one of the first data in the resource and the second data in the forwarding storage element when said determining determines that the first data in the resource and the second data in the forwarding storage element are the same and using the second data from the forwarding storage element when said determining determines that the first data in the resource and the second data in the forwarding storage element are not the same.”

Newly added claims 46-53 are patentable over Olnowich because the reference fails to disclose or suggest at least the above-discussed limitations, as described in more detail below.

The system disclosed in Olnowich includes a memory controller that contains intelligence to decide whether an accessed address is located in a local memory or a remote memory. As specifically indicated in column 8, lines 40-48 of Olnowich:

[t]his is accomplished by comparing memory sector definition bits of the memory address word to the Node ID register. If the compare is equal, the address is located in local memory. In this case, the memory controller accesses and returns the data locally without involving the network adapter. If the compare is not equal, the address is located in remote memory and the memory controller signals the processor that a remote read is required for the thread Z.

In other words the system disclosed in Olnowich determines whether a single address to be accessed is a local address or a remote address. The determination is based on a comparison between the single address to be accessed and the Node ID register (please note column 8, lines 41-48). Once the address is determined to be either a local address or remote address, the address is accessed.

It is readily apparent that the system disclosed in Olnowich is distinct from that of the present invention. Specifically, in the present invention a second processing element accesses data from two locations, i.e., the resource and the forwarding storage element. A comparison is then made between the data accessed from the two locations. If the data is different, the data from one location is used, whereas if the data is the same, the data from either location may be used.

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In other words, the present invention compares data that is accessed from two distinct locations. On the contrary, Olnowich discloses comparing data that is accessed from a single location with a Node ID. Therefore it is clear that Olnowich fails to disclose comparing data that is accessed from two distinct locations. More importantly, Olnowich fails to disclose: that when a second processing element accesses first data in a resource and accesses a second data in a forwarding storage element, and when it is determined that the first data in the resource and the second data in the forwarding storage element are not the same, the second processing element uses the second data from the forwarding storage element, as recited in independent claim 46; or using one of first data in a resource and second data in a forwarding storage element when a determining determines that the first data in the resource and the second data in the forwarding storage element are the same and using the second data from the forwarding storage element when the determining determines that the first data in the resource and the second data in the forwarding storage element are not the same, as recited in independent claim 51.

Under 35 U.S.C. § 102, anticipation requires that each and every element of the claimed invention be disclosed in a prior art reference. *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 U.S.P.Q. (BNA) 303, 313 (Fed. Cir. 1983). In light of *Gore & Associates*, and in light of the above discussion, it is submitted that Olnowich fails to anticipate independent claims 46 and 51 within the meaning of 35 U.S.C. § 102.

Further, because of the differences between that which is recited in independent claims 46 and 51 and that which is disclosed in Olnowich, one of skill in the art at the time of the invention would not have been motivated to modify that which is disclosed in Olnowich to arrive at that which is recited in independent claims 46 and 51. Accordingly, independent claims 46 and 51 are patentable over Olnowich within the meaning of 35 U.S.C. § 103.

Claims 47-50 and 52-53 are dependent upon claims 46 and 51, respectively, and therefore include all the limitations thereof. For this reason, it is additionally submitted that claims 47-50 and 52-53 are patentable over Olnowich. Accordingly, it is respectfully submitted that claims 46-53 are in condition for allowance, an indication of which is requested.

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If there are any outstanding issues that can be resolved by telephone interview, the examiner is asked to call the applicants' attorney Thomas D. Robbins at 202-404-1553.

Kindly charge any additional fees due or credit overpayment of fees to Deposit Account Number 50-0281.

Respectfully submitted,



Thomas D. Robbins
Reg. No. 43,369
Associate Counsel (Patents)
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